IN THE CLAIMS:

Please amend the claims as indicated in the complete listing of claims provided below.

1-19 (Canceled)

20. (Currently Amended) An execution unit in a microprocessor comprising:

a plurality of look-up tables;

a first circuit coupled to the plurality of look-up tables, the first circuit configured to receive a string of bits;

a second circuit coupled to the plurality of look-up tables and the first circuit, the second circuit configured to receive a plurality of data elements, in response to the microprocessor receiving a single instruction, the second circuit generating a plurality of indices using the plurality of data elements and the string of bits, wherein a first one of the plurality of indices is generated from retrieving a first bit segment from the string of bits according to a first one of the plurality of data elements,

the plurality of look-up tables looking up simultaneously a plurality of entries using the plurality of indices; and

a third circuit coupled to the plurality of look-up tables, the third circuit combining the plurality of entries into a first result.

21. (Original) An execution unit as in claim 20 further comprising:

a fifth circuit coupled to the second circuit, the fifth circuit configured to receive at least one format; and

a sixth circuit coupled to the fifth circuit and the third circuit, in response to the microprocessor receiving the single instruction,

the fifth circuit formatting the string of bits into at least one escape data using the at least one format, and

the sixth circuit combining the at least one escape data with the first result into a second result.

22. (Previously Presented) A processing system comprising a plurality of execution units including an execution unit as in claim 21.

23-85 (Canceled)

86. (Previously Presented) An execution unit as in claim 20 wherein the third circuit combines the plurality of entries into the first result before a result based on the first result is outputted into an entry of a register file.

87. (Canceled)

88. (Currently Amended) An execution unit as in claim [[87]] 20 wherein a second one of the plurality of indices is generated from retrieving a second bit segment from the string of bits according to a second one of the plurality of data elements; and the first bit segment of the string of bits and the second bit segment of the string of bits have different bit lengths.

89. (Previously Presented) An execution unit as in claim 20 wherein the string comprises a plurality of variable length codes; and the plurality of data elements specify bit lengths of the variable length codes.

90. (Canceled)